

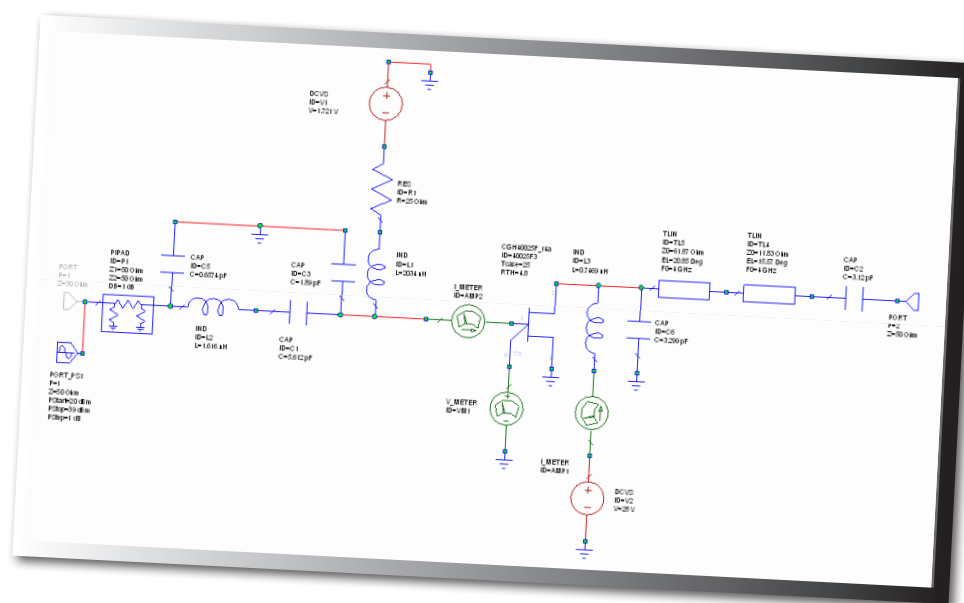
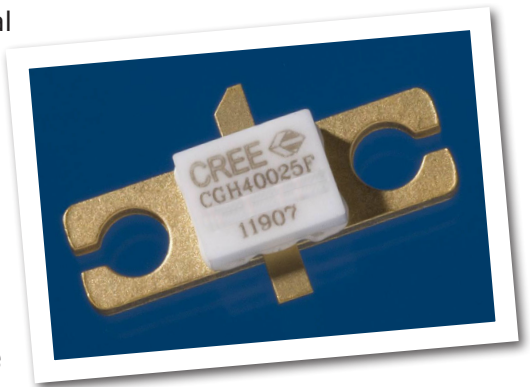
APPLICATION NOTE

Thermal Optimization of GaN HEMT Transistor Power Amplifiers Using New Self-heating Large-signal Model

INTRODUCTION

Gallium nitride power transistors have very high RF power densities which range from 4 to 12 watts per millimeter of gate periphery depending on operating drain voltage. Even though GaN/AlGaIn on SiC substrates have high thermal conductivity, it is necessary to be aware of channel temperature rise incurred by both DC and RF stimuli when designing power amplifiers. Thermal management is even more important for broadband amplifiers (a very popular application) where drain efficiencies can vary considerably as a function of frequency.

A new self-heating feature in Cree's GaN HEMT large-signal models automatically effects both DC and RF parameters as a function of transistor drawn current. We will use the CGH40025F transistor in a 2 to 6 GHz broadband amplifier and demonstrate how the transistor operating temperature can be minimized during the simulation phase of the design. The default thermal resistance is set for the CGH40025F at 4.8°C/watt. The operating case temperature (T_{case}) is user defined. The self-heating engine automatically calculates the rise in temperature (T_{rise}) of the HEMT channel above T_{case} .



T_{rise} can be used as a function of other parameters such as frequency, output power and efficiency. The paper shows the direct lowering of T_{rise} using optimization in unison with the maintenance of output power. Such thermal optimization assures reliable operation as well as improved performance since the transistors are operating cooler.

Application Note: APPNOTE-006 Rev. A

BASIC AMPLIFIER DESIGN

2 GHz TO 6GHz DEMONSTRATION AMPLIFIER SIMULATION

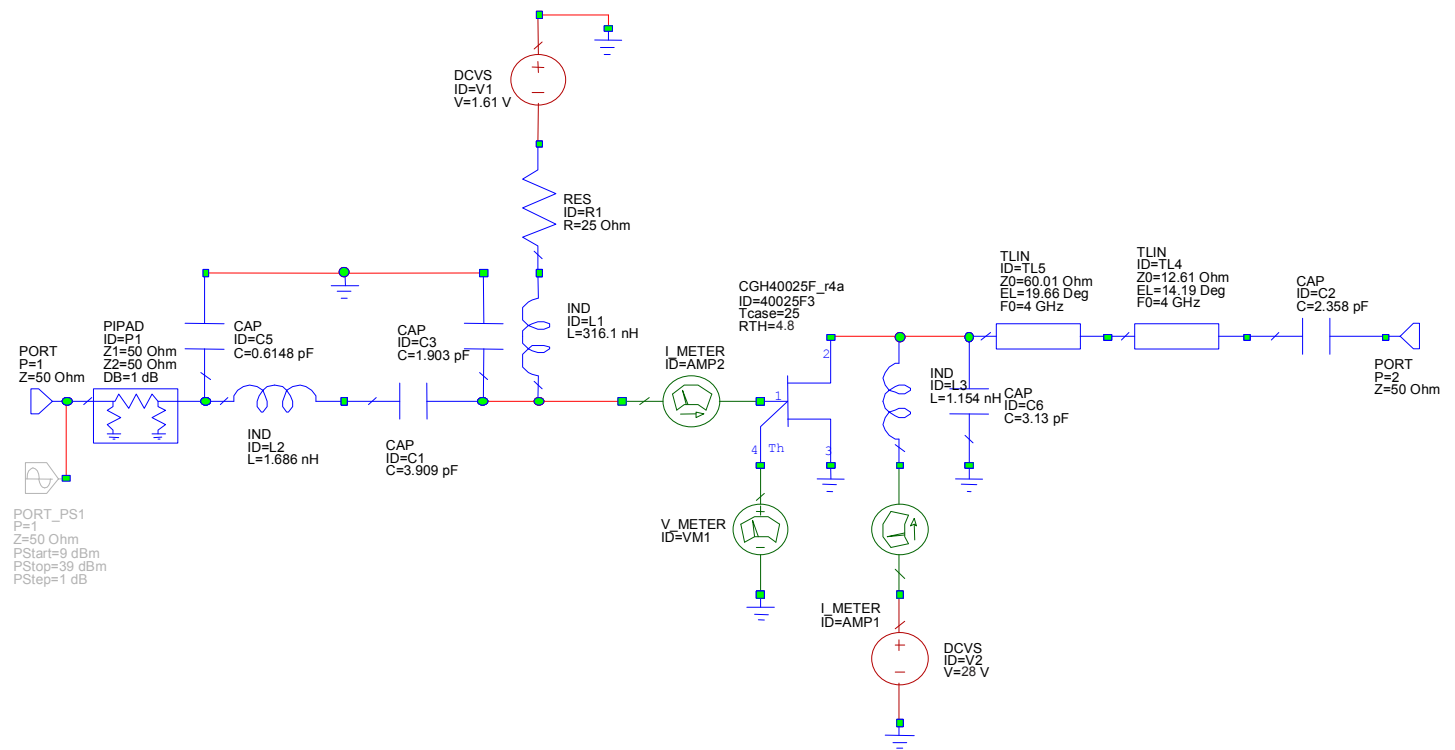


Figure 1 - 2 to 6 GHz, 25 W Broadband PA Schematic

Figure 1 shows the basic schematic of a broadband, 2 to 6 GHz, power amplifier utilizing a Cree CGH40025F GaN HEMT transistor. This device operates from a nominal 28 volt rail. The transistor symbol in the schematic shows a 4 port device – gate, drain, source and temperature monitor – a voltmeter serves as the “thermometer”.

Initial circuit design was concentrated on achieving broadband and flat small signal gain across the wanted frequency range (Figure 2). The power transfer characteristics of the amplifier were then simulated. For example, at a constant CW input power of 38 dBm the output power is plotted as a function of frequency in Figure 3 where it can be seen that the output power varies somewhat due to different levels of compression and impedance match.

SIMULATED PERFORMANCE PRIOR TO OPTIMIZATION

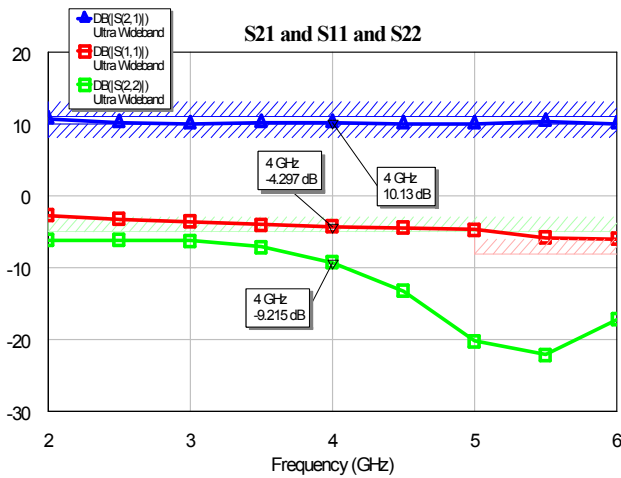


Figure 2 - S21, S11 and S22 prior to optimization

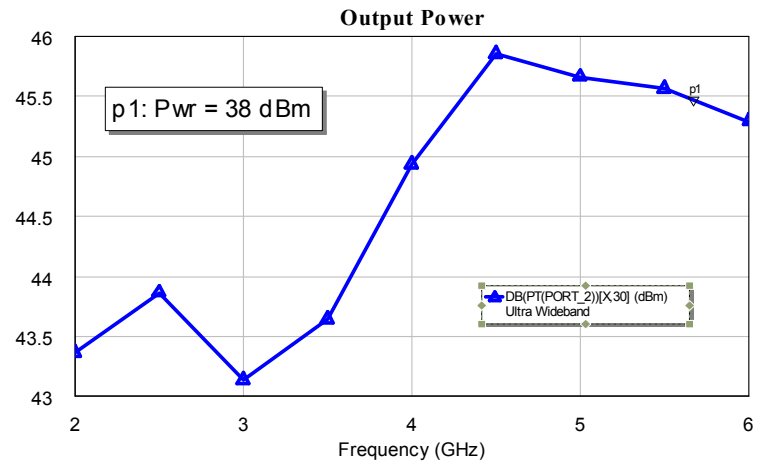


Figure 3 - Output Power vs. frequency at Pin=38 dBm prior to optimization

The self-heating feature of the large-signal model automatically calculates the thermal rise in the transistor from package flange to channel. This is shown in Figure 4 for the amplifier before any specific attention has been taken to decreasing operating drain current. Optimization parameters were set up in Microwave Office for output power, gain and temperature rise as a function of frequency. The intention of the optimization is to ensure that the transistor's channel temperature never exceeds 225°C at a case temperature of 80°C i.e. a temperature rise of 120°C.

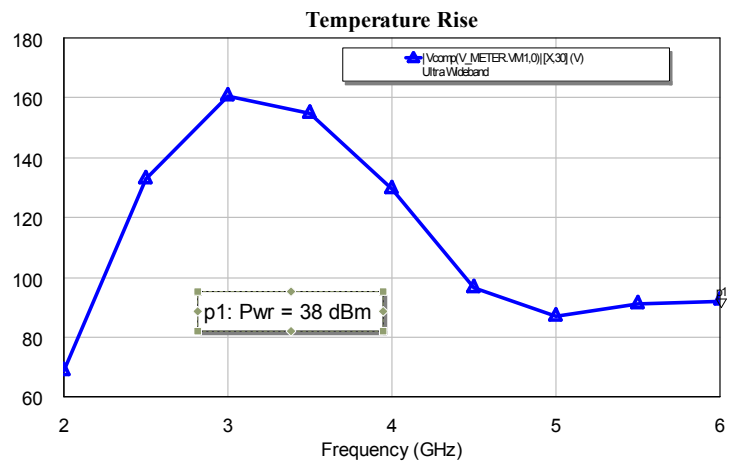


Figure 4 - Transistor temperature rise above T_{case} prior to optimization



SIMULATED PERFORMANCE AFTER TO OPTIMIZATION

Following thermal optimization the small signal parameters are re-simulated as shown in Figure 5 where there is little change in gain and some improvement in output return loss. Figure 6 shows the CW output power as a function of frequency – again there is general improvement in output power over the band even though the “profile” has changed.

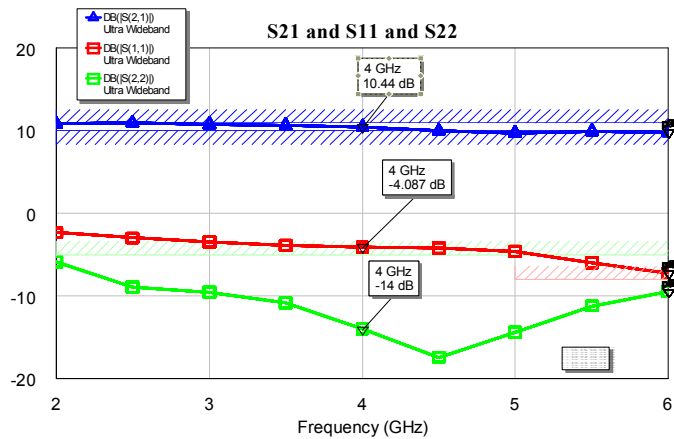


Figure 5 - S21, S11 and S22 after optimization

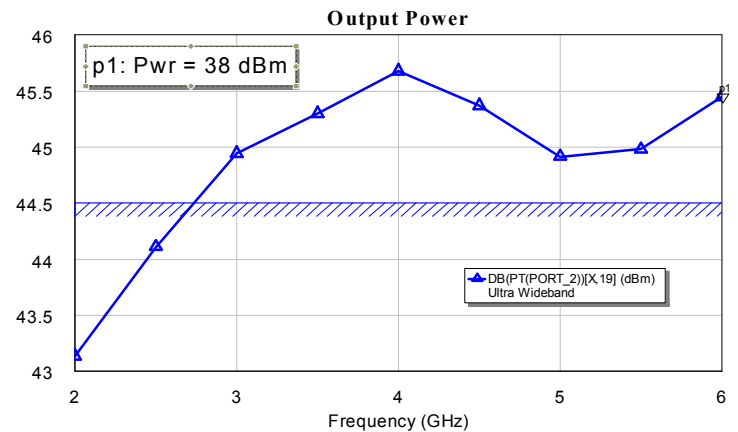


Figure 6 - Output Power vs. frequency at Pin=38 dBm after optimization

Figure 7 is a plot of transistor drain current as a function of frequency which indicates drain current reduction of as much as 20% compared to the original design. Figure 8 indicates the temperature rise after thermal optimization showing temperature decreases of as much as 40°C compared to the original design (the thermal optimization boundary can be clearly seen in this figure).

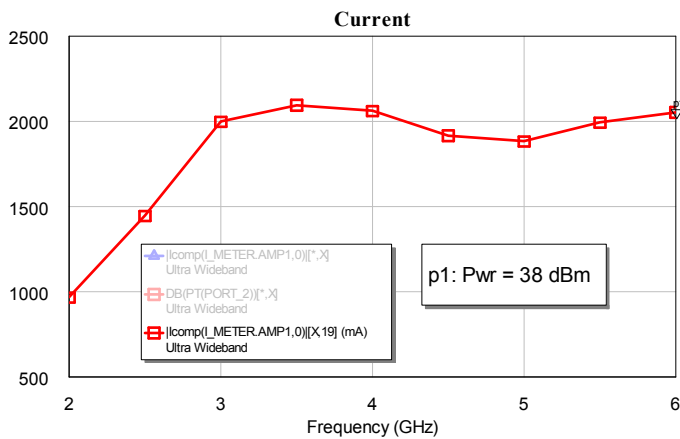


Figure 7 - Drain current vs. frequency at Pin of 38 dBm after optimization

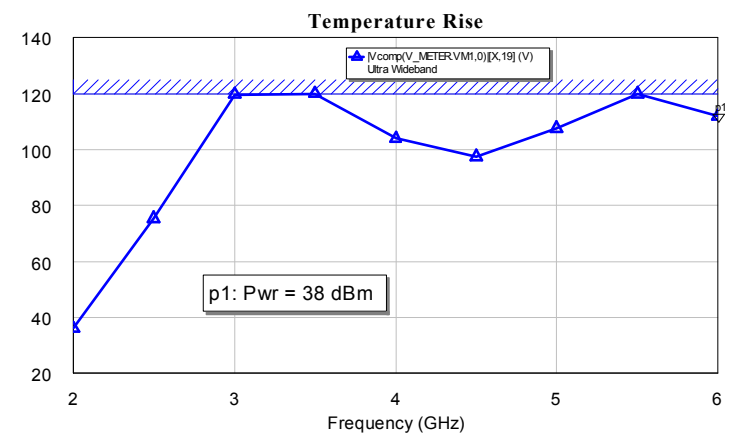


Figure 8 - Transistor temperature rise above T_{case} after optimization



CONCLUSION

This paper has shown the first published demonstration of how to use the new self-heating feature of Cree's large-signal GaN HEMT models to calculate transistor temperature rise as a function of other parameters such as frequency and RF power level. Specifically the self-heating engine has been used, via optimization, to lower transistor temperature by minimizing T_{rise} while maintaining output power.

REFERENCE

Cree, Inc. proprietary large-signal model CGH40025F_r4a for Applied Wave Research's Microwave Office generated the results in this application note.