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Advances in high power GaN HEMT transistors

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Gallium nitride (GaN) HEMT based power transistors are fast becoming adopted for many high power amplifier applications from CW to pulsed or modulated requirements. The key advantage of GaN HEMT transistors for high power amplifiers is their exceptionally high operating power density. Cree's GaN HEMT devices are capable of running at RF power densities as high as 8 W/mm of gate periphery due to their superior thermal properties which are provided by the silicon carbide substrates on which they are fabricated. This is of considerable advantage when compared with silicon substrates. The recently released family of 120 W power transistors from Cree is an excellent example of the advantages of GaN HEMTs and the SiC based materials system. Examples of three different power transistors covering a wide range of applications will be examined in this article.

Figure 1a (top, left): Modeled DC-IV curves for unit cell model — Figure 1b (bottom left and right): Measured and modeled small signal plots for unit cell model — Figure 1c (top, right): Measured and modeled load-pull contours for unit cell model.

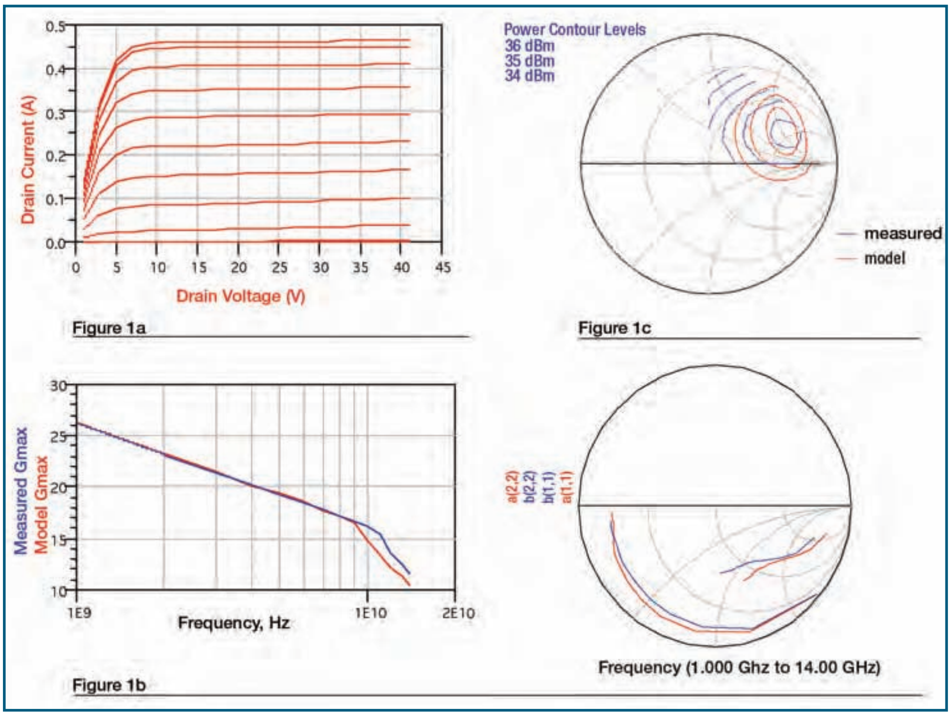

Figure 1a

Figure 1c

Figure 1b

A new family of high power GaN HEMT transistors

The CGH40120F is a 120 W, highly efficient GaN HEMT microwave transistor for general-purpose military and industrial applications such as homeland security, tactical communications, radar, EMC and DVB. The CGH40120F consists of a single un-matched GaN HEMT device providing over 120 W of saturated power in a small, industry-standard ceramic-metal package. The exceptional performance of the transistor has been demonstrated in a number of amplifier applications including a 1200 to 1400 MHz instantaneous bandwidth reference amplifier that offers greater than 18 dB typical small-signal gain, 100 W typical CW output power, and typical power added efficiencies of 75 percent over the entire band. Power amplifiers, operating at 28 V, have also been demonstrated over the 800 to 1300 MHz frequency range for tactical data link applications with output powers of greater than 90 W at efficiencies greater than 65 percent and for digital video broadcast (DVB) applications at 1450 MHz frequency band where, at an average output power of 40 W under 16QAM OFDM, the device provides 19 dB gain at a power back-off efficiency of 40 percent.

The unmatched general purpose CGH40120F is complemented by two pre- matched, 120 W, highly efficient, GaN HEMT microwave transistors for telecommunication applications such as W-CDMA, LTE and WiMAX. The new transistors, CGH21120F and CGH25120F, consist of single, input pre-matched GaN HEMT devices providing over 120 W of saturated power in small, industry-standard ceramic-metal packages. These transistors offer user friendly input and output impedances allowing very convenient device matching over greater than 30 percent instantaneous bandwidths.

The CGH21120F is designed to be used primarily in the 1800 to 2300 MHz frequency range while the CGH25120F is optimized for the 2300 to 2700 MHz range — this allows the same transistors to be used for DCS (GSM), PCS (GSM and CDMA), W-CDMA, WiMAX, WiBro and LTE. Two demonstration amplifiers — one for each device — are available for transistor evaluation. For example, the CGH21120F provides over 110 W of peak CW power at 70 percent efficiency with a gain of 16 dB. Under W-CDMA 3GPP stimulus the transistor provides 20 W average power with 35 percent efficiency in straightforward Class A/B operation. This is the highest W-CDMA efficiency available from any commercial transistor of this power level at this frequency.

Transistor design and modeling

All of these new power transistors use the same 28.8 mm gate width die which is based upon a 0.72 mm unit cell which also forms the basic building block of Cree's large signal models. The model for this high periphery die is scaled by a factor of 40:1! To be successful in scaling by such a large ratio it is imperative that the unit cell model be extremely well correlated with measured data in all regions of operation. Figure 1 shows a comparison of measured and modeled data in all three critical domains, DC-IV, small signal, and large signal behavior.

With an accurate and scalable large signal model in place it is then possible to design much large power transistors. The next critical aspect of power transistor modeling is that of package modeling. A physically derived modeling approach to the package parasitic interconnects has been developed which consists of a number of different tools including s-parameter measurements of package elements, EM simulations and quasi-static wire-bond models.

A cross section of a pre-matched package device model is shown in Figure 2 indicating the different techniques used in the generation of the package model. The reference planes of the package model are also indicated in this figure. It is important to note that since the reference planes for such package models are usually defined immediately at the package body any subsequent circuit modeling must take into account the physical distance that exists between the printed circuit board trace and the package body. The effect of any ground plane discontinuities should also be taken into account. This becomes particularly important when using large power transistors with low input and output impedances at high frequencies greater than 2 GHz.

Amplifier design

The general design technique for all of these high power amplifiers is to first load-pull the transistor model within a harmonic balance simulator such as Microwave Office. Care has to be taken to ensure that the transistor does not become unstable in this unmatched environment otherwise the source and load pull will either give incorrect values or simply not converge. The source and load impedances then form the basis for initial circuit design (ref. 1). Once the initial circuits are synthesized the complete amplifier is simulated, optimized and refined. Finally a completely model driven layout with all required electromagnetic (EM) blocks is used to generate the circuit board layout.

A number of CGH40120F based amplifiers have been designed using a common printed circuit board approach. A single frequency match to the transistor's source and load impedances were determined using Smith chart matching to provide a starting point for the optimization of the input and output matching networks (ref. 1). The networks were then optimized to give better than -20 dB return loss across the desired bandwidth. This was achieved by allowing the capacitors to “slide” along the fixed transmission lines with varying values as required. No more than 6 elements were optimized simultaneously to ensure that the optimizer was able to rapidly converge on a solution. Once the initial networks were designed the complete amplifier was optimized to achieve the desired performance goals. Finally any optimized capacitor values were reset to standard values to ensure that the amplifier could be assembled using available standard capacitors. A schematic and associated layout showing how the simulation was setup to “slide” the capacitors is shown in Figure 3.

A number of amplifiers have been designed using the CGH40120F transistor over the frequency bands and applications shown in Table 1. The predicted key performance characteristics for each of these designs are also shown. The transistor has also been shown to work exceptionally well in pulsed applications.

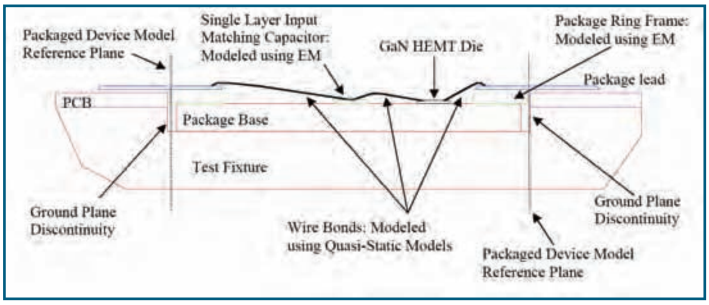

Figure 2: Cross section of a typical pre-matched power transistor showing different modeling techniques and reference plane issues.

TSMC rolls sign-off flow, RF design kit

Seeking to accelerate the product development process, Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) is rolling out a one-two punch in the arena: it has unveiled a mixed-signal/RF design kit as well as a foundry-specific integrated sign-off flow.

TSMC's bigger announcement appears to be the so-called Integrated Sign-Off Flow, which is a turnkey EDA flow. The flow consists of specific and pre-qualified EDA and IP tools from multiple vendors, which are selected by the foundry giant. Customers must still buy the EDA tools from the third-party vendors. But because the flow has been qualified and tuned for TSMC's fabs, chip makers can bring a product to the market more rapidly by following the pre-defined and strict guidelines in the process.

The initial flow from TSMC (Hsinchu, Taiwan) is available for 65-nm designs. The new flow shortens the design cycle and improves tape-out quality, said Tom Quan, deputy director of design services marketing at TSMC. “It's an executable flow,” Quan said. “We know there are a lot of people struggling with their own flows. We can help them.”

For years, the silicon foundry giant and its rivals have offered a design reference flow, which consists of various third-party EDA, DFM, IP and other tools. The flow provides a suggested guideline or path to enable a particular design.

In this model, chip makers must continue to evaluate and buy a complex raft of EDA, DFM and IP tools. This reference flow model works, but chip designs continue to get more complex and expensive.

To help customers, TSMC is taking another approach. Its Integrated Sign-Off Flow is a complete RTL-to-GDSII chip implementation flow. It consists of the exact and process-specific items, including pre-qualified libraries, IP and selected EDA tools.

There are some advantages in going this route. This is especially true for chip makers with lack of resources in their CAD departments. In its new flow, TSMC selects the EDA tools, as opposed to the chip maker itself. This in turn saves time and money. “It takes an enormous amount of time to evaluate the tools,” Quan said.

The disadvantage is a chip maker is tied to specific tools or design methodologies. The flow consists of several different pieces. Synopsys provides the place and route tools. Synopsys and Cadence Design Systems provide the signoff timing analysis (STA) tools. Apache Design Solutions provides the electromigration (EM) and related tools. Mentor Graphics and Cadence provide the DFM products. And Azuro supports the clock-tree products.

The flow is not for all chip makers. “Large fabless companies are early adopters,” Quan said. “They have their own flows.”

On the other hand, some large chip makers could also go the “sign-off flow” route. Quan added the flow could also be geared for a “second wave” of customers, many of which are still devising new 65-nm designs.

The timing could be ripe for such an offering. Amid a major downturn, the silicon foundry industry is expected to see a rally in the second quarter — and perhaps beyond.

Right now, major foundry vendors — Chartered, TSMC, SMIC and UMC — are all seeing a rebound after a huge drop in orders. The surge could be a replenishment cycle in the channels — or a real upturn — or a combination or both. More likely, it's somewhere in the middle.

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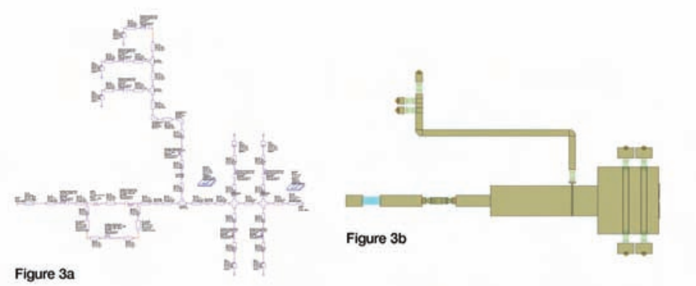
Figure 3a: Simulation schematic of typical input matching network for the CGH40120F — Figure 3b: Simulation layout of typical input matching network for the CGH40120F.



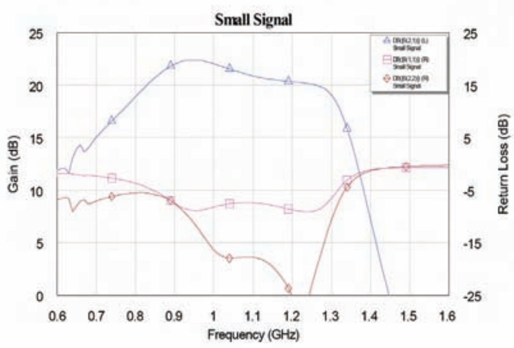


Figure 4a: Small signal simulation of CGH40120F in 800 to 1300 MHz amplifier.

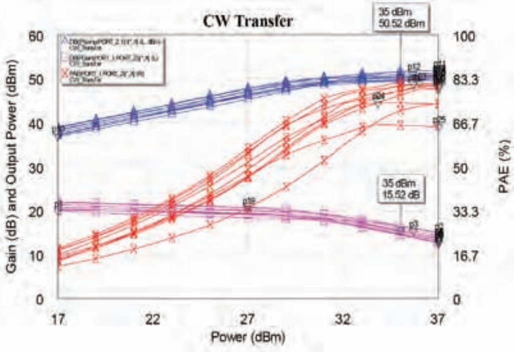
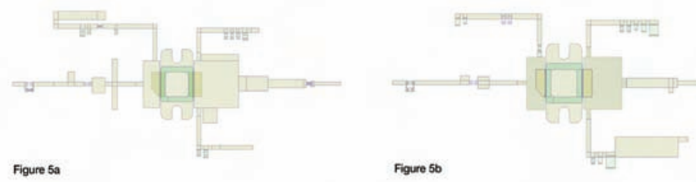


Figure 4b: Large signal simulation of CGH40120F in 800 to 1300 MHz amplifier.

Figure 5a: Simulation layout of CGH21120F based amplifier — Figure 5b: Simulation layout of CGH25120F based amplifier.



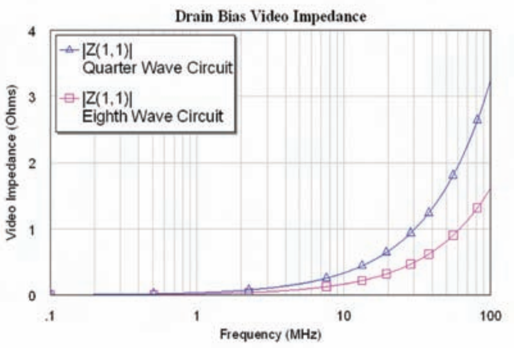


Figure 6: A comparison of traditional quarter-wave and foreshortened bias feeds at video frequencies.

Full circuit simulations of both small and large signal performances of the 800 to 1300 MHz amplifier design are shown in Figure 4.

The telecommunication amplifiers, using both the CGH21120F and the CGH25120F, were designed using a distributed matching technique with transmission lines to implement the input and output networks. This approach was used since these designs operate at higher frequencies, albeit at slightly reduced bandwidths, where the parasitic effects of via inductance and capacitor resonances are much more difficult to model accurately. The amplifier designs for the two transistors are able to cover many different applications due to the inherent power bandwidth of these GaN HEMT devices. Table 2 lists the different telecommunication bands that can be covered with one amplifier design for each transistor.

These amplifiers were also designed using layout driven simulation — the complete model based amplifier layouts are shown in Figure 5. When designing high Q and effectively "narrow band" designs with GaN HEMTs it is important to have performed sufficient stability analyses to prove that any designed amplifiers will not oscillate once assembled. Typically, there are three key techniques used to stabilize GaN HEMT devices in narrow band amplifier designs: a high pass, low frequency stabilization network in series with the input match, a series resistive gate feed, or series stabilization resistance in the RF input path close to the device. These techniques can easily be identified in the layouts.

These designs are optimized for maximum peak power and efficiency while maintaining high gain at typical average power levels. Since these amplifiers must meet stringent linearity requirements it is widely accepted, that for average powers greater than 20 W, digital pre-distortion will be applied to ensure that the requisite linearity can be achieved with high peak to average power ratios while not compromising efficiency at backed-off power levels. While the amplifier linearity may not be a key design parameter careful attention is kept on absolute distortion levels. This ensures that any commercially available digital pre-distortion solution may be applied and provide compliance to spectral masks and EVM requirements.

One important design aspect for wide bandwidth linear systems is to ensure that the bias feeds to the amplifier provide low impedance, resonant free response at video frequencies (ref. 2, 3 and 5). Video bandwidth is broadly defined as being frequencies up to three times the signal bandwidth. When dealing with instantaneous signal bandwidths of 20 MHz the 60 MHz video bandwidth becomes

Table 1: A comparison of CGH40120F based amplifier designs using a single PCB.

Frequency Band (GHz)	Applications	Output Power (W)	Gain (dB)	Efficiency (%)
0.8 – 1.3	LTE, GSM, cdmaOne, Link16	100	18	65
1.4 – 1.5	DVB-H	40 (Ave.)	18.5	40
0.8 – 1.0	GSM	120	20	75

Table 2: Telecommunication standards covered with the CGH21120 and CGH25120 based high power amplifiers.

Device	Frequency Band (GHz)	Applications
CGH21120F	1.8 – 2.3	cdmaOne cdma2000 W-CDMA HSDPA (FDD) TD-SCDMA LTE
CGH25120F	2.3 – 2.7	WiBro 802.16e WiMAX HSDPA (FDD) TD-SCDMA LTE DVB-H

a challenging design task (ref. 4)! Figure 6 shows the difference in response between a simple quarter wave feed and a foreshortened feed. It is important to note that although the foreshortened feed has better response at video frequencies it does not have optimal performance at microwave frequencies. With this observation it follows that the foreshortened feed becomes an integral part of the output network design.

The final simulated amplifier performances for both telecommunication transistors are shown in Figures 7 and 8. These amplifiers were predicted to have exceptional performance over many different telecommunication bands.

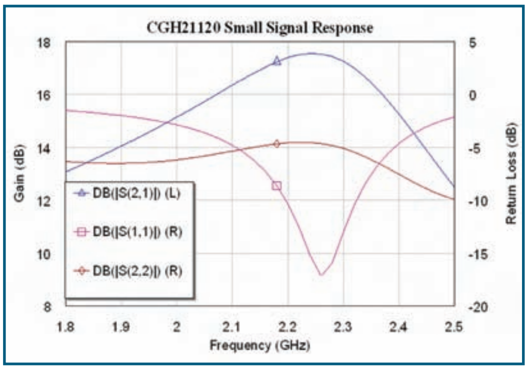


Figure 7a: Small signal simulation of CGH21120F test board.

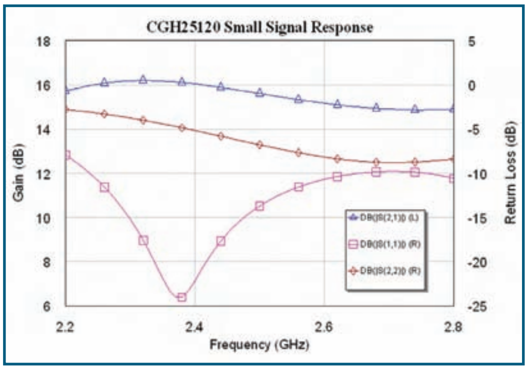


Figure 7b: Small signal simulation of CGH25120F test board.

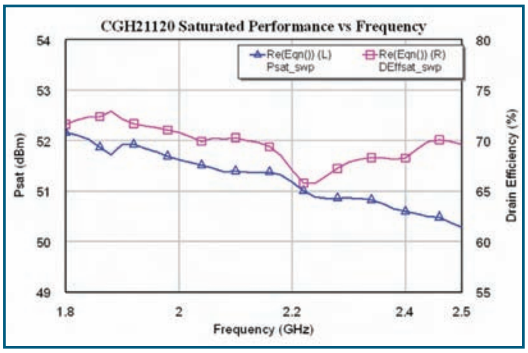


Figure 8a: Large signal simulation of CGH21120F test board.

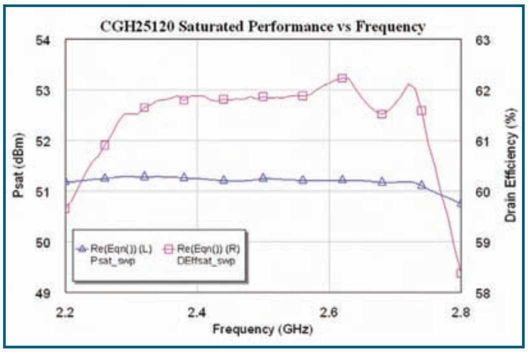


Figure 8b: Large signal simulation of CGH25120F test board.

Elonics secures additional $1.1 million equity finance

As market demand increases for Elonics products, investors have contributed a further $1.1m to develop the sales and operational support infrastructure now required for its growing global customer base. The top-up investment comes from the same group involved in the company's series A funding round for £2.5m ($5m) in February and June 2008. Key investors include Braveheart Investment Group, Scottish Venture Fund and a number of private investors.

Elonics, founded in 2003, has achieved a breakthrough in RF tuner technology, solving the perennial problem of combining high performance with low power and cost. The company's patented DigitalTune™ radio tuner chip platform, designed in CMOS, significantly improves signal path management and can be easily configured to support worldwide industry standards and frequencies for a wide number of applications. Its latest RF tuner, the E4000 focuses on mobile phone and home consumer electronics markets where DigitalTune™ is a key enabling technology for a new generation of TV receivers.

The market for flexible tuner chips for mobile devices and consumer electronics is predicted to grow rapidly over the next few years. Elonics has a comprehensive patent portfolio and a growing product range in development that places the company in a strong position.

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AWR adds TriQuint devices to Microwave Office software

AWR has announced that users of the company's Microwave Office design software now have access to XML library data for a broad array of microwave amplifiers from TriQuint Semiconductor's San Jose design center (formerly WJ Communications). The devices include packaged gain-blocks, FETs, and heterojunction bipolar transistor (HBT) amplifiers.

The library provides measurement-based models and footprints used for printed circuit board (PCB) and module layouts. It is available to users of AWR's Microwave Office software through the XML library link accessible from the software. While the majority of the library is targeted for small signal simulation, many nonlinear models are available for the AP60x Series high-voltage HBT amplifiers. The data sheet for each TriQuint device can be viewed by clicking the "Vendor Help" button from within the Microwave Office parameter dialog box for the device, which connects the user directly to TriQuint's website.

These new XML parts increase both the volume and quality of AWR's rapidly-growing vendor parts. The library is available from the AWR website www.awrcorp.com, and other vendors can add and modify parts within AWR's vendor program as TriQuint has done.

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Measured amplifier performance and applications examples

The next section of this article shows the measured performance of some of the amplifiers described above. It can be seen in all cases that the measured results agree closely with simulated performance parameters. The first results shown are for two different amplifiers designed with the CGH40120F transistor. Figure 9 shows the instantaneous broad band power performance of the transistor — of particular note is the exceptional PAE attained. The amplifier has better than 60 percent PAE over almost 50 percent bandwidth. The second amplifier was optimized for use in a DVB (digital video broadcast) application at 1.45 GHz. DVB uses high peak to average QAM modulation which can be challenging in terms of amplifier performance due to the amount of back-off which is needed. Figure 10 shows the CGH40120F at 40 W of average output power. At this power level the amplifier's power added efficiency was 40 percent and the ACP is shown to be -33 dBc.

The second set of results in Figures 11 and 12, show the performance of the CGH21120F based amplifier. This amplifier was designed for operation under W-CDMA modulation in the UMTS frequency band of 2.11 to 2.17 GHz. Figure 11a shows the typical power performance measured under pulsed conditions. A typical efficiency of 70 percent is maintained across a very wide bandwidth as shown in Figure 11b. The performances of the amplifier under single and multi-carrier W-CDMA are shown in Figures 12a and 12b respectively. In the single carrier measurement, at 25 W average output power, the amplifier corrects under DPD by greater than 25 dB with an

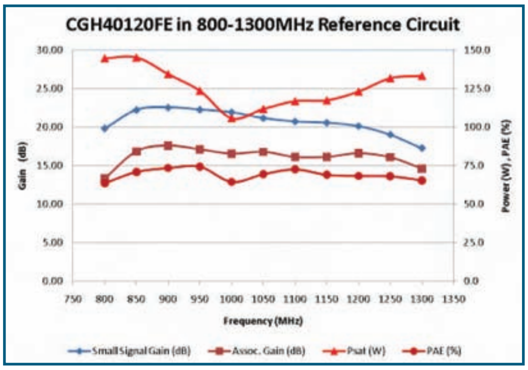


Figure 9: Measured data for CGH40120F in broad-band 800 – 1300 MHz design.

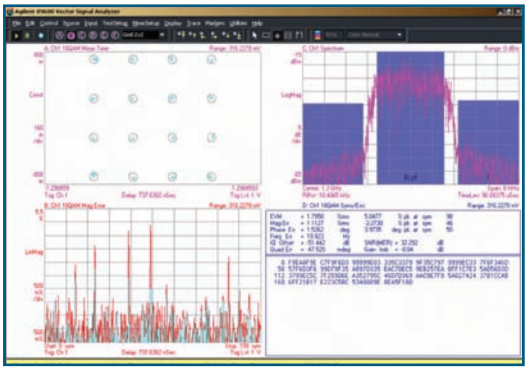


Figure 10: Measured linearity data for the CGH40120F at 40 W average under 16-QAM OFDM for 1.45 GHz DVB-H applications.

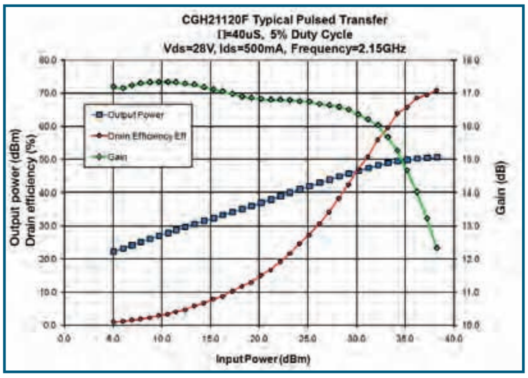


Figure 11a: Pulsed transfer characteristics for CGH21120F at 2.14 GHz.

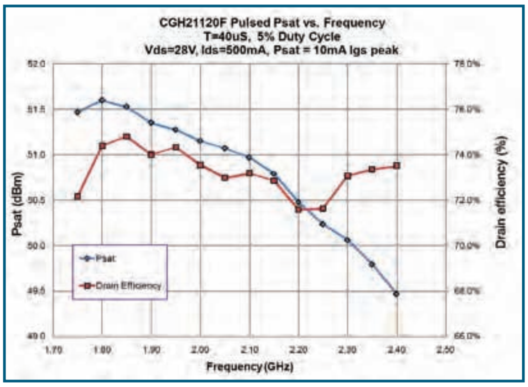


Figure 11b: Pulsed transfer characteristics for CGH21120F versus frequency.

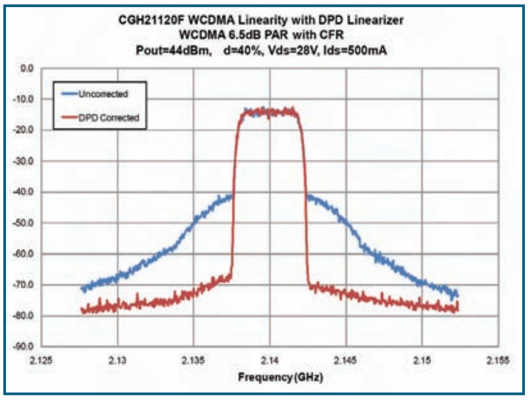


Figure 12a: Digital pre-distortion correction of a single W-CDMA carrier centered at 2.14 GHz using the CGH21120F-TB.

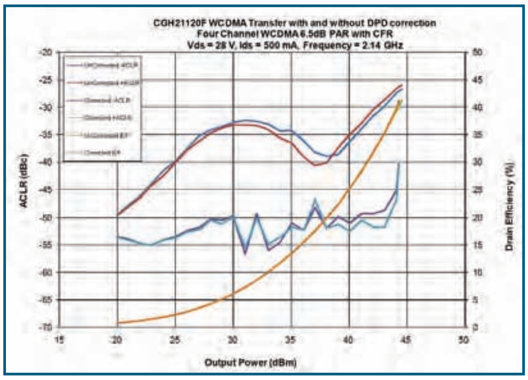


Figure 12b: Digital pre-distortion correction of a 4 carrier W-CDMA signal centered at 2.14 GHz using the CGH21120F-TB

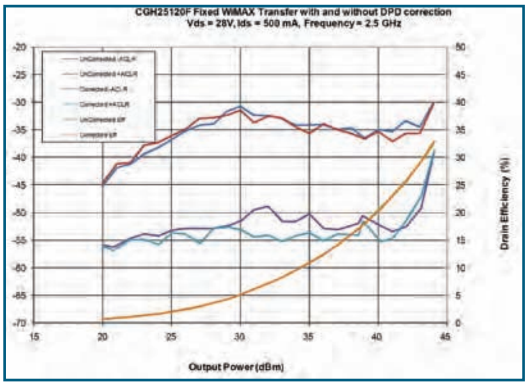
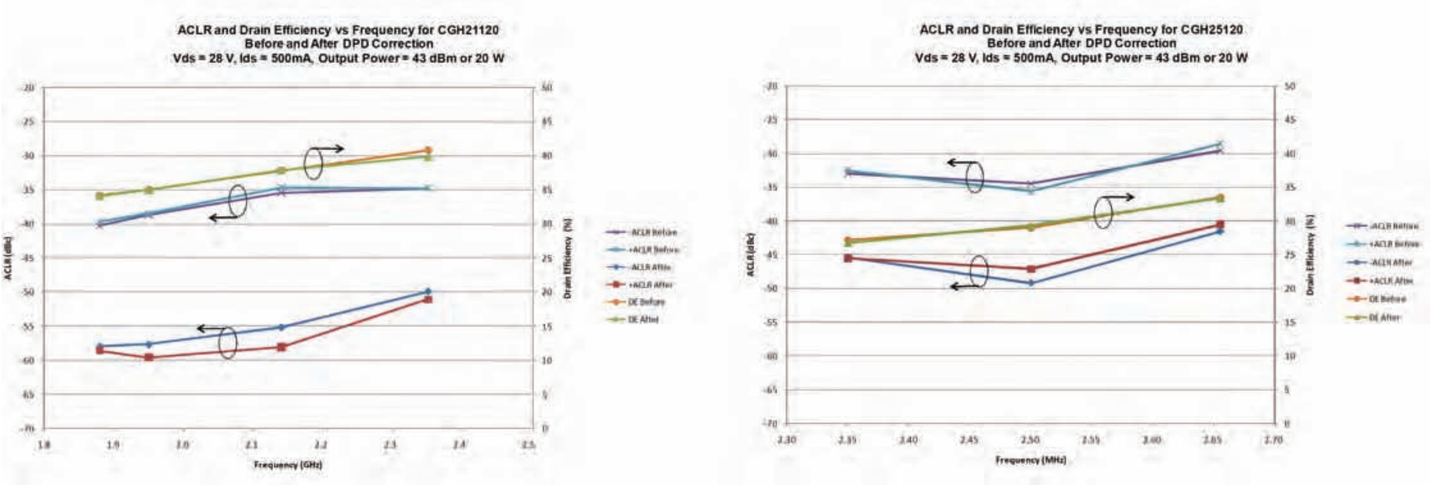


Figure 13: Digital pre-distortion correction of a 10MHz WiMAX carrier centered at 2.5 GHz using the CGH25120F-TB

Figure 14: Digital pre-distortion of CGH21120F and CGH25120 at 20 W average output power covering applications from 1.8 GHz to 2.7 GHz with only 2 transistors.



accompanying efficiency of 40 percent. This level of correction is also maintained under 4-carrier excitation. The 20 MHz wide multicarrier signal places great emphasis on the video bandwidth of the amplifier (ref. 4).

Figure 13 shows that the CGH25120F is also capable of being corrected when under more stringent WiMAX modulation. The signal personality used in conjunction with the Optichron DPD system is fully compliant to 802.16e WiMAX with a PAR of 11.5 dB. It can be seen that at 20 W average output power the amplifier corrects beyond the -45 dBc spectral emissions mask (SEM) point at 1.5 MHz removed from the carrier edge (6.5 MHz from center on this 10 MHz signal). At this average power level the efficiency is 30 percent. Figure 14 shows the results for digital pre-distortion correction at other frequencies for both the CGH21120F-TB and CGH25120F-TB amplifiers.

Summary and Conclusions

A new family of high power GaN HEMT power transistors have been introduced with exceptionally high performance. This article has described many of the challenges in creating large signal models. Detailed descriptions of various amplifier design approaches employing a variety of newly available, high power GaN HEMT transistors, covering 800 MHz to 2700 MHz, was given. Table 3 shows a summary of the performance measured for each amplifier.

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Device	Frequency Band (MHz)	Applications	Output Power (W)	Gain (dB)	Efficiency (%)
CGH40120F	800 – 1300	Link16	100	18	65
	1400 – 1500	DVB-H	40 (Ave.)	18.5	40
CGH21120F	1880 1950 2140	W-CDMA	25 (Ave.)	15	40
CGH25120F	2350 2500 2655	802.16e WiMAX	20 (Ave.)	13	30

Table 3: Performances of all 120 W GaN HEMT transistor based high power amplifiers.